

Appl. No. 09/607,815
Amdt. Dated August 17, 2005
Reply to Office Action of May 17, 2005

Listing of the Claims:

1. (Currently Amended) A method of operating a processor to repeatedly execute an instruction, comprising:
determining at run time how many times a single instruction is to be repeated;
loading at run time an existing general purpose register with a count value
indicative of the number of times a single instruction is to be executed;
fetching and executing a REPEAT instruction, the REPEAT instruction indicating the single instruction to be repeatedly re-executed;
fetching the single instruction; and
repeatedly executing the single instruction for a consecutive number of times as indicated by the count value without refetching the single instruction and without adding a NOP (no operation) instruction.

2. (Currently Amended) A method of operating a processor to repeatedly execute an instruction comprising:
fetching a REPEAT instruction;
executing a REPEAT instruction, wherein execution of the REPEAT instruction determines and stores at run time in a an existing general purpose register a count value indicative of the number of times a single instruction is to be executed;
fetching the single instruction; and
repeatedly executing the single instruction consecutively for as many times as indicated by the count value without re-fetching the single instruction and without fetching any other instruction and without adding a NOP (no operation) instructions;
decrementing the count value in the register each time the single instruction is executed; and
incrementing a program counter once the count value in the register is one or less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle.

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3. (Currently Amended) A method of operating a processor to repeatedly execute an instruction comprising:

determining at run time a count value indicative of how many times a single instruction is to be repeated;

loading at run time a general purpose register with [[a]]the count value indicative of the number of times a single instruction is to be executed;
fetching and executing a REPEAT instruction indicating the single instruction that is to be repeatedly executed;

incrementing a program counter;

fetching the single instruction;

repeatedly executing the single instruction for as many times as indicated by the count value stored in the register without refetching the single instruction and without fetching any other instruction and without adding a NOP (no operation) instruction;

decrementing the count value stored in the register each time the single instruction is executed; and

stalling the program counter until the count value in the register is one or less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle.

4. (Original) A method of operating a processor according to claim 3, wherein said count value is stored in said count register before execution of said REPEAT instruction.

5. (Canceled)

6. (Original) A method of operating a processor according to claim 3,

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wherein said method further comprises:

incrementing the program counter after the single instruction has been executed
for as many times as indicated by the count value.

7. (Original) A method according to claim 3, wherein method further
comprises:

decrementing said count value stored in said register each time said single
instruction is executed; and
determining whether said count value is less than or equal to zero.

8. (Currently Amended) A processor for repeatedly executing a single
instruction, said processor comprising:

means for determining at run time a count value indicative of how many times
a single instruction is to be reapeated;

means for loading at run time a general purpose register with [[a]]the count
value indicative of the number of times the single instruction is to be executed;
means for fetching a REPEAT instruction, the REPEAT instruction indicating
the single instruction to be repeatedly executed;

means for executing the REPEAT instruction indicating the single instruction
to be repeatedly executed;

means for fetching the single instruction; and

means for repeatedly executing the single instruction a consecutive number of
times as indicated by the count value without refetching the single instruction without adding
a NOP (no operation) instruction.

9. (Currently Amended) A processor for repeatedly executing an
instruction, comprising:

means for determining at run time how many times a single instruction is to be

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repeated:

means for fetching a REPEAT instruction;

means for executing a REPEAT instruction, wherein execution of the REPEAT instruction at run time stores in a general purpose register a count value indicative of the number of times a single instruction is to be executed;

means for fetching the single instruction;

means for repeatedly executing the single instruction for as many times as indicated by the count value without re-fetching the single instruction and without fetching any other instruction without adding a NOP (no operation) instruction;

means for decrementing the count value in the register each time the single instruction is executed; and

means for incrementing a program counter once the count value in the register is less than zero, thereby providing an effective data rate of one transfer every clock cycle.

10. (Currently Amended) A processor for repeatedly executing an instruction, comprising:

means for determining at run time how many times a single instruction is to be repeated:

means for loading a general purpose register at run time with a count value indicative of the number of times a single instruction is to be executed;

means for fetching a REPEAT instruction indicating the single instruction that is to be repeatedly executed;

means for executing the REPEAT instruction indicating the single instruction that is to be repeatedly executed without adding a NOP (no operation) instruction;

means for incrementing a program counter;

means for fetching the single instruction; and

means for repeatedly executing the single instruction for a consecutive number of times as indicated by a count value stored in a count register without refetching the single

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instruction and without fetching any other instruction;
means for decrementing the count value stored in the register each time the single instruction is executed; and
means for incrementing a program counter once the count value in the register is equal to zero, thereby providing an effective data rate of one transfer every clock cycle.

11. (Original) A processor according to claim 10, wherein said count value is stored in said count register before execution of said REPEAT instruction.

12. (Canceled)

13. (Original) A processor according to claim 10, wherein said processor further comprises:
means for incrementing the program counter after the single instruction has been executed for as many times as indicated by the count value.

14. (Original) A processor according to claim 10, wherein processor further comprises:
means for decrementing said count value stored in said register each time the single instruction is executed; and
means for determining whether said count value is less than or equal to zero.

15. (Currently Amended) A processor for repeatedly executing one or more processor instructions, said processor comprising:
a memory address register associated with a main memory;
a memory data register associated with the main memory;
a memory control for generating memory control signals;

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a program counter for storing a memory address location of the main memory where an instruction is to be fetched;

an instruction register for storing an instruction that is to be executed;

at least one general purpose register for storing a count;

decode and execute control logic for decoding and executing an instruction stored in the instruction register; and

a state machine for controlling the fetching and repeated execution of a single instruction, the state machine configured to repeatedly execute the single instruction by signaling the instruction register to hold the same instruction and not fetch the next instruction without refetching the single instruction and to decrement the count stored in the general purpose register each time the single instruction is executed, and to signal the program counter not to increment until increment the program counter once the count stored in the general purpose register is below a threshold value, thereby providing an effective data rate of one transfer every clock cycle.

16. (Cancelled)

17. (Original) A processor according to claim 15, wherein said general purpose register includes a first register for storing a count value indicative of the number of times the single instruction is to be repeatedly executed.

18. (Original) A processor according to claim 17, wherein said state machine generates signals for decrementing the count value stored in the first register.

Claims 19-22 (Cancelled)

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23. (Currently Amended) The method of operating a processor to repeatedly execute an instruction of claim 15, further comprising wherein the state machine is configured to increment[[ing]] the program counter once the count value is equal to zero.

24. (Currently Amended) The method of operating a processor to repeatedly execute an instruction of claim 15, further comprising the state machine configured to increment[[ed]] the program counter once the count value is less than zero.

25. (Cancelled)

26. (Previously Presented) The processor for repeatedly executing a single instruction of claim 8, further comprising means for incrementing a program counter once the count value is equal to zero.

27. (Previously Presented) The processor for repeatedly executing a single instruction of claim 8, further comprising means for incrementing a program counter once the count value is less than zero.

28. (Previously Presented) The processor for repeatedly executing a single instruction of claim 8, wherein a program counter remains unchanged as the single instruction is repeatedly executed.

29. (Previously Presented) The method of operating a processor to repeatedly execute an instruction of claim 2, wherein the program counter remains unchanged as the single instruction is repeatedly executed.

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30. (Previously Presented) The method of operating a processor to repeatedly execute an instruction of claim 2, wherein the program counter is effectively stalled on the single instruction.

31. (Previously Presented) The method of operating a processor to repeatedly execute an instruction of claim 3, wherein the program counter remains unchanged as the single instruction is repeatedly executed.

32. (Previously Presented) The method of operating a processor to repeatedly execute an instruction of claim 3, wherein the program counter is effectively stalled on the single instruction until the single instruction executes the number of times indicated by the count value.